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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/836,777	04/17/2001	Gary D. Martin	AMCC-002XX	6860

207 7590 11/30/2004

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EXAMINER	
MEW, KEVIN D	
ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/836,777	MARTIN, GARY D.	
	Examiner	Art Unit	
	Kevin Mew	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-8 and 10-12* is/are rejected.

7)☒ Claim(s) *5, 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

In particular, the abstract's word count is 154 words, which is slightly above the maximum length of 150 words. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 6-8, 10-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Irwin et al. (USP 5,841,771).

Regarding claim 1, a SONET multiplexed communications system (see Fig. 6) comprising:

at least one SONET input signal path configured to receive at least one input signal (input data transmission path, see col. 6, lines 18-48 and Fig. 6);

at least one SONET output signal path configured to transmit at least one output signal corresponding to the input signal (output data transmission path, see col. 6, lines 18-48 and Fig. 6); and

a time slot interchange circuit operatively coupled between the SONET input and output signal paths (time slot switch module is provided for serial communication between input and output data transmission paths, see col. 6, lines 18-20) and configured to provide time division multiplexed connections for the input and output signals (the switch module includes an intermediate data transmission path consisting of a plurality of parallel data conduits for being operated in the TDM format, see col. 6, lines 18-29),

wherein the SONET input signal path includes a pointer interpreter (input controller maintains N pointer, see col. 15, lines 64-67 and col. 16, lines 6-9) configured to interpret at least one input signal pointer (N pointer is read pointer which defines the next of the queues in the buffer for reading a cell payload) serially coupled to a synchronization buffer (cell buffer 460, see Fig. 6) configured to transfer the input signal from a respective clock rate of the SONET input signal path to a respective clock rate of the time slot interchange circuit (input data transmission path is operated at a rate defined by a timing signal and a frame signal, wherein the frame signal occurs once with each occurrence of a predetermined plurality of occurrences of the timing signal, to define frames of time slots in a time division multiplex format in the switch module, see col. 6, lines 49-60), and

wherein the SONET output signal path includes a pointer generator (input controller maintains M pointer, see col. 15, lines 64-67 and col. 16, lines 2-5) configured to generate at least one output signal pointer (M pointer is write pointer which defines the next empty storage location into which the payload is to be written, see col. 16, lines 2-5) serially coupled to a first-in first-out buffer (cell buffer 460 is a FIFO buffer, see col. 15, lines 28-33 and Fig. 6) configured to transfer the output signal from the respective clock rate of the time slot interchange circuit (time switch module) to a respective clock rate of the SONET output signal path (output data transmission path is operated at a rate defined by a timing signal and a frame signal, wherein the frame signal occurs once with each occurrence of a predetermined plurality of occurrences of the timing signal, to define frames of time slots in a time division multiplex format in the switch module, see col. 6, lines 49-60).

Regarding claim 2, the system of claim 1 wherein the pointer interpreter SONET precedes the synchronization buffer in the SONET input signal path (the input controller precedes the cell buffer 460, see Fig. 6).

Regarding claim 3, the system of claim 1 wherein the synchronization buffer precedes the pointer interpreter in the SONET input signal path.

Regarding claim 4, the system of claim 1 wherein the input signal STS-M (M > 1) signal (see col. 10, lines 42-47), and SONET input signal path (see Fig. 6) further includes an alignment buffer (multiplexer 411, Fig. 6) operatively coupled between the synchronization buffer (cell

buffer 460) and the time slot interchange circuit (elements 424, 428, 429, 422, Fig. 6) and configured to perform column alignment on the STS-M signal (the multiplexer performs the alignment in which each channel on the incoming lines is assigned a predetermined fixed time location with the high-speed SONET frame stricture, see col. 10, lines 42-65).

Regarding claim 6, the system of claim 1 wherein the at least one SONET input signal path comprises plurality of SONET input signal paths and the least one SONET output signal path comprises plurality of SONET output signal paths (see col. 6, lines 49-54), the number of SONET input signal paths being greater than the number of SONET output signal paths (see the number of input lines 415 is greater than the number of output line 413c, Fig. 6).

Regarding claim 7, a SONET multiplexed communications system (see Fig. 6), comprising:

at least one SONET input signal path configured to receive at least one input signal (input data transmission path, see col. 6, lines 18-48 and Fig. 6);

at least one SONET output signal path configured to transmit at least one output signal corresponding the input signal (output data transmission path, see col. 6, lines 18-48 and Fig. 6);

at least one time slot interchange circuit operatively coupled between SONET input and output signal paths (time slot switch module is provided for serial communication between input and output data transmission paths, see col. 6, lines 18-20) and configured provide time division multiplexed connections for the input and output signals (the switch module includes an

intermediate data transmission path consisting of a plurality of parallel data conduits for being operated in the TDM format, see col. 6, lines 18-29),

wherein the SONET input signal path (see Fig, 6) includes synchronization buffer (cell buffer 460, see Fig. 6) is configured to transfer input signal from a respective clock rate SONET input signal path to a respective clock rate of the time slot interchange circuit (input data transmission path is operated at a rate defined by a timing signal and a frame signal, wherein the frame signal occurs once with each occurrence of a predetermined plurality of occurrences of the timing signal, to define frames of time slots in a time division multiplex format in the switch module, see col. 6, lines 49-60; note that elements 424, 428, 429, 422 in Fig. 6 are interpreted as part of the time slot interchange circuit), and

wherein the SONET output signal path includes a pointer interpreter (input controller maintains N pointer, see col. 15, lines 64-67 and col. 16, lines 6-9) configured interpret at least input signal pointer (N pointer is read pointer which defines the next of the queues in the buffer for reading a cell payload), pointer generator (input controller maintains M pointer, see col. 15, lines 64-67 and col. 16, lines 2-5) configured generate at least one output signal pointer (M pointer is write pointer which defines the next empty storage location into which the payload is to be written, see col. 16, lines 2-5), and a first- in first-out buffer (cell buffer 460 is a FIFO buffer, see col. 15, lines 28-33 and Fig. 6) serially coupled between the pointer interpreter and the pointer generator (cell buffer 460 is serially coupled to input controller 480, see Fig. 6) and configured transfer the output signal from respective clock rate of the time interchange circuit respective clock rate of the SONET output signal path (input and output data transmission paths are operated at a rate defined by a timing signal and a frame signal, wherein the frame signal

occurs once with each occurrence of a predetermined plurality of occurrences of the timing signal, to define frames of time slots in a time division multiplex format in the switch module, see col. 6, lines 49-60).

Regarding claim 8, the system of claim 7 wherein the input signal STS-M (M > 1) signal (see col. 10, lines 42-47), and SONET input signal path (see Fig. 6) further includes an alignment buffer (multiplexer 411, Fig. 6) operatively coupled between the synchronization buffer (cell buffer 460) and the time slot interchange circuit (elements 424, 428, 429, 422, Fig. 6) and configured perform column alignment on the STS-M signal (each channel on the incoming lines is assigned a predetermined fixed time location with the high-speed SONET frame stricture, see col. 10, lines 42-65).

Regarding claim 10, the system of claim 7 wherein the at least one SONET input signal path comprises plurality of SONET input signal paths and the least one SONET output signal path comprises plurality of SONET output signal paths (see col. 6, lines 49-54), the number of SONET input signal paths being greater than the number of SONET output signal paths (see the number of input lines 415 is greater than the number of output line 413c, Fig. 6).

Regarding claim 11, a method operating SONET multiplexed communications system (see Fig. 6), comprising the steps of:

receiving at least one input signal by at least one SONET input signal path (input data transmission path receives a plurality of parallel conduits, see col. 6, lines 18-48 and Fig. 6);

interpreting at least one input signal pointer (N pointer is read pointer which defines the next of the queues in the buffer for reading a cell payload) by a pointer interpreter included the SONET input signal path (input controller maintains N pointer, see col. 15, lines 64-67 and col. 16, lines 6-9);

transferring input signal from a respective clock rate of the SONET input signal path to a respective clock rate a time slot interchange circuit (elements 424, 428, 429, 422, Fig. 6) by synchronization buffer (cell buffer 460, see Fig. 6) included in the SONET input signal path (input data transmission path is operated at a rate defined by a timing signal and a frame signal, wherein the frame signal occurs once with each occurrence of a predetermined plurality of occurrences of the timing signal, to define frames of time slots in a time division multiplex format in the switch module, see col. 6, lines 49-60);

providing time division multiplexed connections for the input signal (defines frames of time slots in a TDM format, see col. 6, lines 18-29) and at least one corresponding output signal by time interchange circuit (time slot interchange circuit outputs signal 413c);

generating at least output signal pointer (M pointer is write pointer which defines the next empty storage location into which the payload is to be written, see col. 16, lines 2-5) by pointer generator included at least one SONET output signal path (input controller maintains M pointer, see col. 15, lines 64-67 and col. 16, lines 2-5);

transferring the corresponding output signal from respective clock rate of the time slot interchange circuit respective clock rate the SONET output signal path (output data transmission path is operated at a rate defined by a timing signal and a frame signal, wherein the frame signal occurs once with each occurrence of a predetermined plurality of occurrences of the timing

signal, to define frames of time slots in a time division multiplex format in the switch module, see col. 6, lines 49-60) by a first-in first-out buffer included in the SONET output signal path (cell buffer 460 is a FIFO buffer, see col. 15, lines 28-33 and Fig. 6); and

transmitting the corresponding output signal by SONET output signal path (transmitting output signal 413c, see Fig. 6).

Regarding claim 12, the method of claim 11 further including the step of performing column alignment input signal by an alignment buffer (multiplexer 411, Fig. 6) included in the SONET input signal path (the multiplexer performs the alignment in which each channel on the incoming lines is assigned a predetermined fixed time location with the high-speed SONET frame stricture, see col. 10, lines 42-65).

Allowable Subject Matter

3. Claims 5 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

In claims 5 and 9, the alignment buffer includes a multitap delay element and a controller circuit, the multitap delay element having an input and a plurality of outputs and being configured receive STS-M signal the input and provide increasingly delayed versions of the STS-M signal at successive ones outputs, controller circuit being configured select a delayed version of the STS-M signal from one outputs application the time interchange circuit.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure with respect to time slot interchanging of time slots from multiple sonet signals without first passing the signals through pointer processors to synchronize them to a common clock.

US Patent 6,778,550 to Blahut

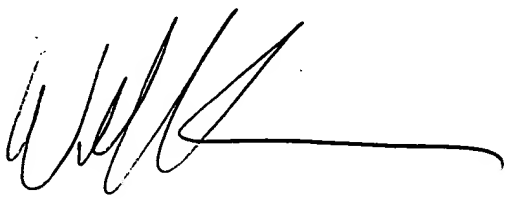
US Patent 6,233,234 to Curry

US Patent 5,812,951 to Ganesan et al.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Mew whose telephone number is 571-272-141. The examiner can normally be reached on 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 571-272-3134. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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